Verilog HDL: Digital Design and Modeling

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Emphasizing the detailed design of various Verilog projects, Verilog HDL: Digital Design and Modeling offers students a firm foundation on the subject matter. The textbook presents the complete Verilog language by describing different modeling constructs supported by Verilog and by providing numerous design examples and problems in each chapter. Examples include counters of different moduli, half adders, full adders, a carry lookahead adder, array multipliers, different types of Moore and Mealy machines, and much more. The text also contains information on synchronous and asynchronous sequential machines, including pulse-mode asynchronous sequential machines.

In addition, it provides descriptions of the design module, the test bench module, the outputs obtained from the simulator, and the waveforms obtained from the simulator illustrating the complete functional operation of the design. Where applicable, a detailed review of the topic's theory is presented together with logic design principles, including state diagrams, Karnaugh maps, equations, and the logic diagram.

Verilog HDL: Digital Design and Modeling is a comprehensive, self-contained, and inclusive textbook that carries all designs through to completion, preparing students to thoroughly understand this popular hardware description language.

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